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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/002,265

Applicant(s)
Van Der Wal

Examiner
Reuben M. Brown

Group Art Unit
2711



☐ Responsive to communication(s) filed on _____

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-30 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-30 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Art Unit: 2711

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 & 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishitani, (U.S. Pat # 4,942,470).

Considering claim 1, the claimed modular video processing system comprising a processing module containing at least one microprocessor which controls hardware and software operation of the video processing system using control data is met by the Nishitani, control unit 300 (Fig. 25; Fig. 26; col. 20, lines 62-68; col. 21, lines 1-42) and command generator 200, (Fig. 18; Fig. 24; col. 16, lines 36-50; col. 20, lines 34-54). The claimed at least one video processing module which contains parallel pipelined video hardware which is programmable by the control data to provide different video processing operations on an input stream of video data is met at

least by the unit processor 3, (col. 20, lines 62-68; col. 7, lines 60-68 thru col. 8, lines 1-65; col. 16, lines 60-65).

Regarding the claimed global video bus which routes video data between the processing module from/to at least one video processing module, Nishitani discloses, with respect to both the fifth embodiment and sixth embodiment, Fig. 18 & Fig. 26, that video data is delivered to each unit processor via BUS2, which leads from terminal 2. Even though these figures, do not explicitly show the origin of terminal 2, it is inherently connected to the processing module or controls, since Nishitani further teaches that the video signal is taken in by input section 10, in response to the write signal from the control unit 300, (col. 21, lines 4-16).

The claimed global control bus which provides control data to/from the processing module from/to at least one video processing module separate from the video data on the global video bus is met at least by the operation of the control unit 300 with respect to terminal 1, as it outputs a sync signal received from terminal 1 to the unit processors, (col. 21, lines 4-9), in the sixth embodiment. With respect to the fifth embodiment, the above limitation is met by the sync signal bus BUS1 and the comma signal from the generator unit 200 which is received at the processing section 11 of the processor units 3-6, (Fig. 18; Fig. 21; col. 18, lines 33-60).

Considering claim 20, the claimed method steps corresponds with subject matter mentioned above in the rejection of claim 1, and is likewise rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson, (U.S. Pat # 5,129,092).

Considering claim 1, the claimed modular video processing system comprising a processing module containing at least one microprocessor which controls hardware and software operation of the video processing system using control data is met by Wilson, controller 27 (Fig. 1; col. 8, lines 49-68; col. 9, lines 1-14). The claimed at least one video processing module which contains parallel pipelined video hardware which is programmable by the control data to provide different video processing operations on an input stream of video data is met by the processor units 10a-10h, (Fig. 2; col. 5, lines 55-65; col. 6, lines 34-53). The claimed global control bus which provides control data to/from the processing module from/to at least one video processing module separate from the video data on the global video bus is met by the clock and control bus 29, (Fig. 1).

Regarding the claimed global video bus which routes video data between the processing module from/to at least one video processing module, Wilson utilized a data input device 20, which serially inputs video data to each processor unit, without using a bus. Official Notice is taken that at the time the invention was made, it was notoriously well known in the art to utilize a common data bus to distribute video data to a plurality of destinations simultaneously. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the well known technique of distribution of video data along a common bus for the known benefit of synchronized delivery of data to a plurality of sources so that the data can be processed simultaneously.

Considering claim 20, the claimed method steps corresponds with subject matter mentioned above in the rejection of claim 1, and is likewise rejected.

5. Claims 2-3, 17 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson, in view of McMullan, (U.S. Pat # 5,550,825).

Considering claim 2, the claimed system wherein video data is coupled with associated video timing information synchronized to a system clock, and each video processing module contains a means which routes video data and its associated video timing information to/from respective parallel pipelined video hardware components such that the timing data is compensated for pipeline delay in the video processing module is provided for by Wilson, (col.

6, lines 5-15), wherein it is disclosed that data is shifted through processor units via shift register, which necessarily requires the use of a timing protocol in order to insure the proper timely delivery of video data to the next stage.

Regarding the claimed limitation of a crosspoint switch , Wilson shows that the output from each processing unit is placed on a bus, generally BUS8. However, Wilson does not detail a crosspoint switch in specific, nevertheless at the time the invention was made it was well known in the art to utilize crosspoint switches in order to route information from a plurality of sources to a plurality of destinations, one such example is shown by McMullan, crosspoint switch 413 (Fig. 4B; col. 8, lines 19-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wilson, with the teachings of McMullan to utilize a crosspoint switch in order to more efficiently transmit/receive data to/from the various buses with which the processor units interface.

Considering claim 3, the claimed crosspoint switch state machine which monitors transfers over each data path of the crosspoint switch is met by the state machine 416, (Fig. 5; col. 10, lines 1-3). Even though the combination of Wilson and McMullan does not explicitly show a process of selecting idle paths for the transfer of data, Official Notice is taken that such an algorithm was well known in the art at the time the invention was made. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of

Wilson and McMullan with the well known technique of selecting a data path which is not in use, for at least the known purpose of avoiding collisions on particular data paths.

Considering claims 17 & 19, the claimed hardware control library which contains a set of functions for programming the video processing unit is met by Wilson, (Abstract), in which it is disclosed that a sequence of instructions are sent to the processing units from the controller. The claimed device information for each video processor is necessarily included in Wilson, the invention operates so that each processor unit may be separately programmed therefore it is necessary that the controller maintain device information on each processor unit so that it knows which functions are provided by which processor unit.

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson and McMullan, in view of Suzuki, (U.S. Pat # 4,400,771).

Considering claim 18, Wilson discloses a system which operates with at least one microprocessor, controller 27. Nevertheless, at the time the invention was made it was well known in the art to utilize, a plurality of microprocessors in order to increase the productivity of the system, since different microprocessors would be enabled to at least operate on different instructions simultaneously. Such a system is taught by Suzuki, (Abstract; Fig. 1; Fig. 2; col. 1,

lines 35-60; col. 2, lines 1-25). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wilson to include at least two microprocessors, as taught by Suzuki, for the known benefit of improving the performance of a microcontrolled system. The claimed step of coordinating multitask operations of the two microprocessors is necessarily included in the combination of Wilson, McMullan & Suzuki.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson and McMullan, in view of van der Wal, (U.S. Pat # 5,359,674).

Considering claim 5, the combination of Wilson and McMullan provide a modular video processing system in which video processors are enabled to perform various functions. However, Wilson does not specifically disclose the function of pyramid processing. Nevertheless, pyramid processing of images was well known in the art at the time the invention was made and is disclosed by van der Wal, (Abstract; Fig. 1; col. 1, lines 5-54; col. 2, lines 3-61). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson and McMullan, to include pyramid processing of video data at different resolutions as taught by van der Wal, for the well known benefit of improving the results of image processing by filtering images according to their resolution.

8. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson and McMullan, in view of Wass, (U.S. Pat # 5,339,221).

Considering claim 6, the combination of Wilson and McMullan discloses a modular video processing system in which a variety video processes are enabled via the various processor units 10a-10h, Wilson (Fig. 1). However, the combination does not particularly disclose the physical component of a daughterboard. Nevertheless, at the time the invention was made, it was well known in the art to utilize daughterboards in order to customize a system which specific functions, see Wass, (Abstract; col. 1, lines 39-48). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson and McMullan to include the teachings of Wass, for the well known purpose of providing a system which can be customized for specific purposes by the user.

Considering claims 7 & 8, the claimed display processor card including video audio connections is met by the combination of Wilson, McMullan and Wass. Even though Wilson only discusses video processing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wilson to include audio processing as well, for the well known purpose of optimizing the audio of a program as well the video. It would have obvious to one of ordinary skill in the art at the time the invention was made to include the feature of decoding and digitizing video data into a predetermined format within a particular daughterboard, according to the teachings of Wilson, McMullan and Wass.

Considering claim 9, Wass teaches the use of at least a LUT feature, however the combination of Wilson, McMullan and Wass do not particularly disclose a CALU and pyramid filter. Nevertheless, Official Notice is taken that such process were well known in the art at the time the invention was made. Therefore using the same logic set forth in the rejection of claim 8 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson, McMullan and Wass to include the features of a pyramid filter and CALU within a daughterboard for the known benefit of a modular video processing system, which fits the specific requirements of the user.

9. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson, McMullan and Wass, in view of Bruehl, (U.S. Pat # 5,051,835).

Considering claims 10 & 11, the cited combination of Wilson, McMullan and Wass discloses a modular video processing system in which a variety video processes are enabled via the various processor units 10a-10h, Wilson (Fig. 1). However, the combination does not particularly disclose a means for enabling a warper function by the video processor. Nevertheless, at the time the invention was made, such a process was well known in the art and is disclosed by Bruehl, (col. 3, lines 29-47). Therefore using the logic set forth in the rejection of claim 8, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson, McMullan and Wass to include the feature of warper card

within a daughterboard for the known benefit of a modular video processing system, which fits the specific requirements of the user. The claimed connections to an address generator and pair of memory banks is met by Wilson, address selector 18 and memory 13 (col. 6, lines 12-33).

10. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson, in view of Suzuki.

Considering claim 12, Wilson discloses a system which operates with at least one microprocessor, controller 27. Nevertheless, at the time the invention was made it was well known in the art at to utilize, a plurality of microprocessors in order to increase the productivity of the system, since different microprocessors would be enabled to at least operate on different instructions simultaneously. Such a system is taught by Suzuki, (Abstract; Fig. 1; Fig. 2; col. 1, lines 35-60; col. 2, lines 1-25). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wilson to include at least two microprocessors, as taught by Suzuki, for the known benefit of improving the performance of a microcontrolled system. The claimed system of having the two microprocessor maintain separate RAM and also access a shared RAM is met by Suzuki, (col. 3, lines 5-30; col. 3, lines 61-38), wherein the memory control unit 23, arbitrates access to memory unit 20, for a plurality of CPU, which necessarily contain their own memory.

Considering claim 13, the claimed synchronous start signal is met by Suzuki (Abstract).

Considering claim 14, the claimed system wherein the processing module further comprises means to communicate with external devices is necessarily included in Wilson and Suzuki.

Considering claim 15, even though Wilson does not specifically show that the memory of the microcontroller 27 is directly connected to the data input device 20, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson and Suzuki to include such an arrangement for the known benefit of synchronized delivery of data to a plurality of sources so that the data can be processed simultaneously.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson and Suzuki, in view of Charles, (U.S. Pat # 5,790,542).

Considering claim 16, the combination of Wilson and Suzuki, introduces a system in which a plurality of microprocessors might be utilized to improve the performance of a modular video processing system. However, a semaphore register is not specifically disclosed. Nevertheless, at the time the invention was made it was well known in the art to utilize semaphore registers in order to exclude the operation of at least one entity from accessing a particular memory area or

application while the instant memory area or application is being accessed by another entity as taught by Charles, (col. 27, lines 1-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson and Suzuki, with the teachings of Charles, for the known benefit of arbitrating access to memory or an application.

12. Claims 1 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau, (U.S. Pat # 5,761,466).

Considering claim 1, the claimed modular video processing system comprising a processing module containing at least one general purpose microprocessor which controls hardware and software operation of the video processing system using control data is met by Chau (Fig. 5; col. 7, lines 60-67 thru col. 8, lines 1-15; col. 8, lines 49-55), wherein the Next PC Logic 74 generates a "next pc" signal which is sent to the microprogram memory storage. The claimed at least one video processing module which contains parallel pipelined video hardware which is programmable by the control data to provide different video processing operations on an input stream of video data is met by the Functional Unit 78, (col. 8, lines 26-55; col. 10, lines 29-50) and Functional Unit 38 (col. 3, lines 1-42).

Regarding the claimed global bus which routes video data between the processing module and the at least one video processing module, the Chau provides that the Functional Units 78 process video data. Even though Chau does not specifically disclose a bus to transmit video data between the microprocessor at least one Functional Unit 78 (video processor), a means for transmitting data to/from the Functional Units 78 is necessary in order to operate Chau. Examiner takes Official Notice, that at the time the invention was made it was well known in the art to transmit data, including video data, from a controlling unit or microprocessor to the various controlled units via a common bus. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chau to include the well known feature of a common data bus for the known benefit of efficiently transmitting the instant data unit to more than one processor simultaneously. The claimed global control bus which provides control data to/from the processing module from/to at least one video processing module separate from the video data on the global video bus is provided in Chau, at least by the global clock control line 76, (Fig. 5; col. 7, lines 60-67). Fig. 5 also shows another global data bus, connecting the Instruction Register 68 and the plurality of Functional Units 78, (col. 8, lines 16-26). This common bus is the not numbered.

Considering claim 20, the claimed method steps corresponds with subject matter mentioned above in the rejection of claim 1, and is likewise rejected.

13. Claims 1 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda, (U.S. Pat # 5,502,512).

Considering claim 1, the claimed modular video processing system comprising a processing module containing at least one general purpose microprocessor which controls hardware and software operation of the video processing system using control data is met by Toyoda control means 105, (Fig. 1; col. 2, lines 49-64; col. 3, lines 25-28; col. 4, lines 31-38). The claimed at least one video processing which contains parallel pipelined video hardware which is programmable by the control data to provide different video processing operations on an input stream of video data is met by the plurality of information input and output processing means 101, 102 and 103 is met by (col. 23, lines 25-50). The claimed global video bus which routes video data between the processing module and the at least one video processing module is met by the bus means 107, (col. 2, lines 61-64; col. 3, lines 15-23). The claimed global control bus which provides control data to/from the processing module from/to separate from the video data on the global video bus is met by the bus means 107. Even though the bus means 107 is depicted as one item, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Toyoda, using the well known technique of putting video data and control data on separate physical lines at least for the known benefit of avoiding interference of signals.

Considering claim 20, the claimed method steps corresponds with subject matter mentioned above in the rejection of claim 1, and is likewise rejected.

14. Claims 2, 4, 20-22, 24-28 & 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda, in view of McMullan.

Considering claim 2, the claimed system wherein video data is coupled with associated video timing information synchronized to a system clock, and each video processing module contains a switch which routes video data and its associated video timing information to/from respective parallel pipelined video hardware components such that the timing data is compensated for pipeline delay in the video processing module is met by Toyoda (Fig. 2; col. 2, lines 25-31; col. 5, lines 14-43).

Regarding the claimed limitation of a crosspoint switch, Toyoda shows that the output from each processing unit is placed on a bus, information transmission means 104. However, Wilson does not detail a crosspoint switch in specific, nevertheless at the time the invention was made it was well known in the art to utilize crosspoint switches in order to route information from a plurality of sources to a plurality of destinations, one such example is shown by McMullan, crosspoint switch 413 (Fig. 4B; col. 8, lines 19-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Toyoda, with the teachings

of McMullan to utilize a crosspoint switch in order to more efficiently transmit/receive data to/from the various buses with which the processor units interface.

Considering claim 4, the claimed means responsive to video data and its timing information to automatically compensate for differences in input timing between respective images is met by Toyoda, (col. 2, lines 26-31).

Considering claims 21 & 28, the claimed method steps which parallel the system elements mentioned above in the rejection of claim 2, are likewise rejected. Regarding the additional limitation of coupling the video timing synchronization information to the global video bus is met by Toyoda, (col. 5, lines 16-24), wherein the synchronized information is sent to the output port 202.

Considering claim 22, the method step of the providing at least one synchronous start signal to the video processors is necessarily included in Toyoda, as it is disclosed that the video processors are synchronized, (col. 2, lines 14-25).

Considering claim 24, the claimed crosspoint switch state machine which monitors transfers over each data path of the crosspoint switch is met by the state machine 416, (Fig. 5; col. 10, lines 1-3). Even though the combination of Toyoda and McMullan does not explicitly show a process of selecting idle paths for the transfer of data, Official Notice is taken that such an

algorithm was well known in the art at the time the invention was made. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Toyoda and McMullan with the well known technique of selecting a data path which is not in use, for at least the known purpose of avoiding collisions on particular data paths.

Considering claims 25 & 30, the claimed device information for each video processor is necessarily included in Toyoda, the invention operates so that each processor unit may be separately programmed therefore it is necessary that the controller maintain device information on each processor unit so that it knows which functions are provided by which processor unit.

Considering claim 26, the claimed method of automatically compensating for differences in input timing between respective images is met by Toyoda, (col. 2, lines 26-31).

Considering claim 27, the claimed elements of a modular processing system which corresponds with elements mentioned above in the rejection of claim 1, are likewise rejected. Regarding the additional limitation of the microprocessor maintaining a hardware control library comprising functions which program the video processor, the input means 106 sends instructions to control means 105, which in turns provides control instructions to each video processor, Toyoda (col. 3, lines 15-28; col. 4, lines 31-39).

15. Claims 23 & 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda and McMullan, in view of Muramatsu, (U.S. Pat # 5,455,920).

Considering claims 23 & 29, Toyoda discloses a system which operates with at least one microprocessor, control means 105. Nevertheless, at the time the invention was made it was well known in the art at to utilize, a plurality of microprocessors in order to increase the productivity of the system, since different microprocessors would be enabled to at least operate on different instructions simultaneously. Such a system is taught by Muramatsu, (Abstract; Fig. 1; col. 2, lines 25-36). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Toyoda and McMullen to include at least two microprocessors, as taught by Muramatsu, for the known benefit of improving the performance of a microcontrolled system. The claimed step of coordinating multitask operations of the two microprocessors is necessarily included in the combination of Toyoda, McMullan and Muramatsu.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A) Kawaguchi, Hillis Parallel Pipelined Video Processing

B) Florentin Warper Card

C) van der Wal, Burt Pyramid filter processing

Any response to this action should be mailed to:

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reuben M. Brown whose telephone number is (703) 305-2399. The examiner can normally be reached on Monday thru Friday from 830am to 430pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Faile, can be reached on (703) 305-4380. The fax phone number for this Group is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.


ANDREW I. FAILE
SUPERVISORY PATENT EXAMINER
GROUP 2700